RF2137

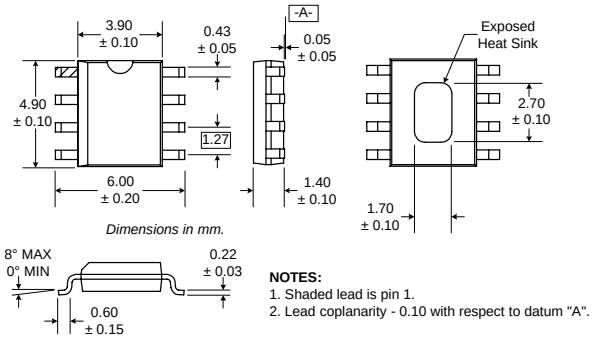
LINEAR POWER AMPLIFIER

Typical Applications

- 4.8V AMPS Cellular Handsets
- 4.8V CDMA/AMPS Handsets
- 4.8V JCDMA/TACS Handsets
- Driver Amplifier in Cellular Base Stations
- Portable Battery-Powered Equipment

Product Description

The RF2137 is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 4-cell CDMA/AMPS hand-held digital cellular equipment, spread spectrum systems, and other applications in the 800MHz to 950MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics at all recommended supply voltages.



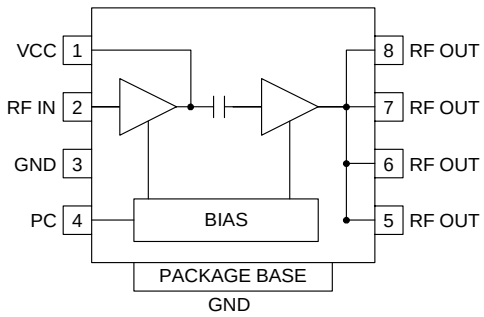
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: SOIC-8 Slug

Features

- Single 4.2V to 6.0V Supply
- Up to 29 dBm Linear Output Power
- 27dB Gain With Analog Gain Control
- 45% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 950MHz Operation



Functional Block Diagram

Ordering Information

RF2137	Linear Power Amplifier
RF2137 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (No RF)	-0.5 to +8.0	V_{DC}
Supply Voltage (P_{OUT}<31dBm)	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +6.0 or V_{CC}	V
DC Supply Current	800	mA
Input RF Power	+12	dBm
Output Load VSWR	10:1	
Ambient Operating Temperature	-30 to +90	℃
Storage Temperature	-40 to +150	℃

Refer to “Handling of PSOP and PSSOP Products” on page 16-15 for special handling information.

Caution! ESD sensitive device.

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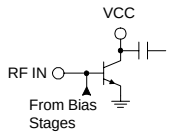
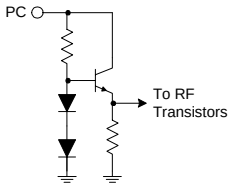
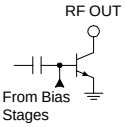
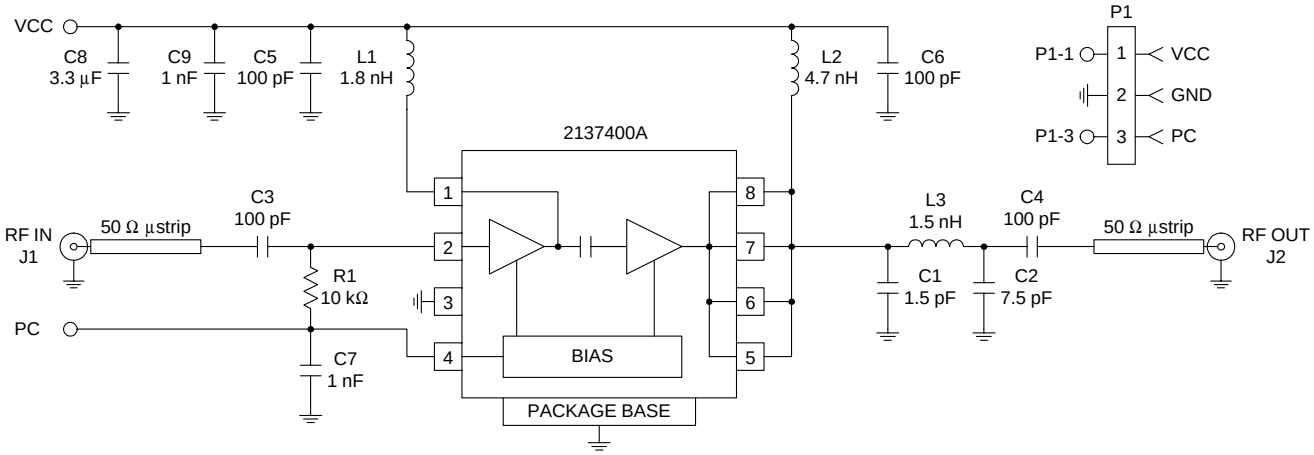
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25℃, V_{CC}=5.0 V, V_{PC}=3.6V, Freq=824MHz to 849MHz
Usable Frequency Range	800	824 to 849	950	MHz	
Linear Gain	25	27	29	dB	
Total Linear Efficiency	40	45		%	
Efficiency at Max Output	50	55		%	
OFF Isolation		27		dB	V_{PC}=0V,P_{IN}=+6dBm
Second Harmonic		-30		dBc	Including Second Harmonic Trap
Maximum Linear Output Power		28.5	29	dBm	IS-95A CDMA Modulation
Adjacent Channel Power @ 885kHz offset		-46	-44	dBc	Pout = 28 dBm ACPR can be improved by trading off efficiency.
Adjacent Channel Power @ 1.98MHz offset		-58	-56	dBc	Pout = 28 dBm
Max CW Output Power	31.5	+32.0		dBm	
Input VSWR		<2:1			
Output Load VSWR			10:1		No oscillations
Power Down					
Turn On/Off Time			100	ns	
Total Current			10	µA	“OFF” State
V_{PC} “OFF” Voltage	0.2		0.5	V	Threshold Voltage at Input
V_{PC} “ON” Voltage	3.6		Vcc	V	Threshold Voltage at Input
Power Supply					
Power Supply Voltage	4.2	5.0	6.0	V	Operating voltage
Idle Current		40	100	mA	V_{PC}=4.0V
Current into VPC pin		15	20	mA	

Pin	Function	Description	Interface Schematic
1	VCC	Power supply for the driver stage, and interstage matching. Shunt inductance is required on this pin, which can be achieved by an inductor to V_{CC}, with a decoupling capacitor on the V_{CC} side. The value of the inductor is frequency dependent; 3.3nH is required for 830MHz, and 1.2nH for 950MHz. Instead of an inductor, a high impedance microstrip line can be used.	
2	RF IN	RF input. This is a 50Ω input, but the actual input impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
4	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V or less at room temperature. During normal operation this pin is the power control. Control range varies from about 2V for 0dBm to V_{CC} for +31dBm RF output power. The maximum power that can be achieved depends on the actual output matching. PC should never exceed 6.0V or V_{CC}, whichever is lowest.	
5	RF OUT	RF Output and power supply for the output stage. The three output pins are combined, and bias voltage for the final stage is provided through these pins. The external path must be kept symmetric until combined to ensure stability. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
6	RF OUT	Same as pin 5.	See pin 5.
7	RF OUT	Same as pin 5.	See pin 5.
8	RF OUT	Same as pin 5.	See pin 5.
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device may be required.	

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
1.559" X 1.191"